FIG. 1
CONVENTIONAL ART

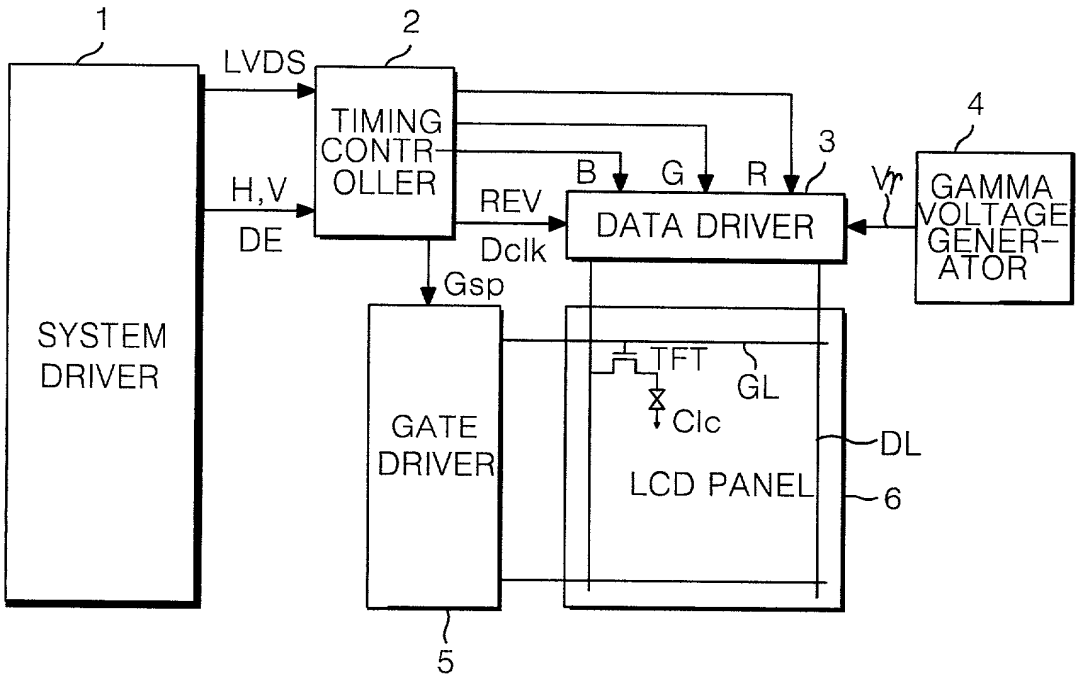


FIG.2
CONVENTIONAL ART

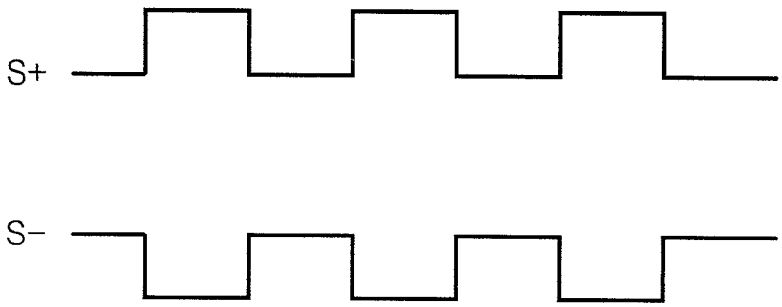


FIG.3
CONVENTIONAL ART

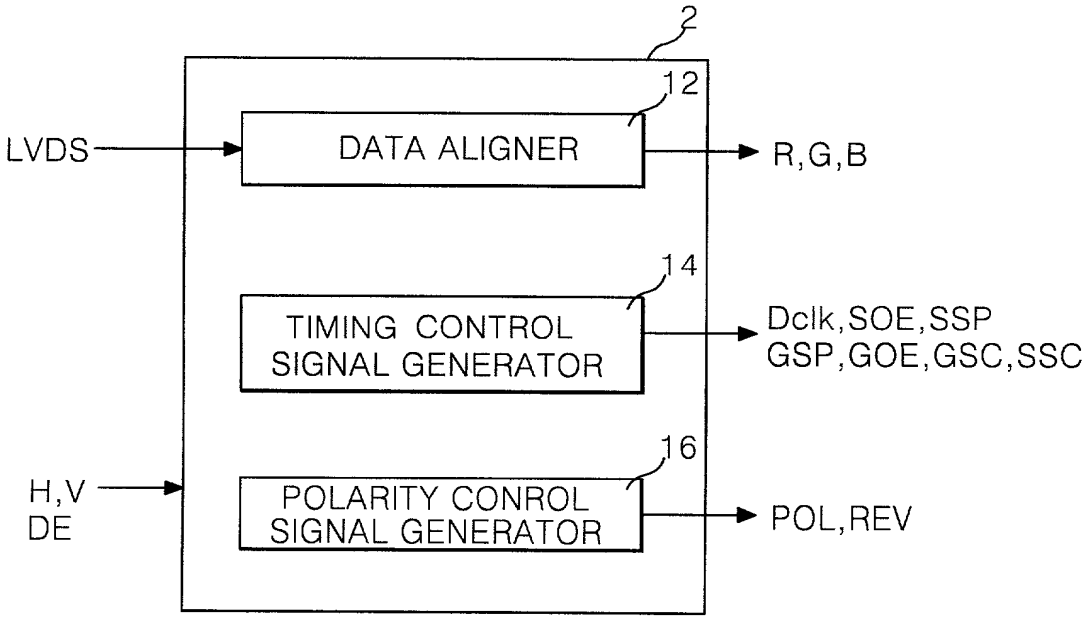


FIG. 4A
CONVENTIONAL ART

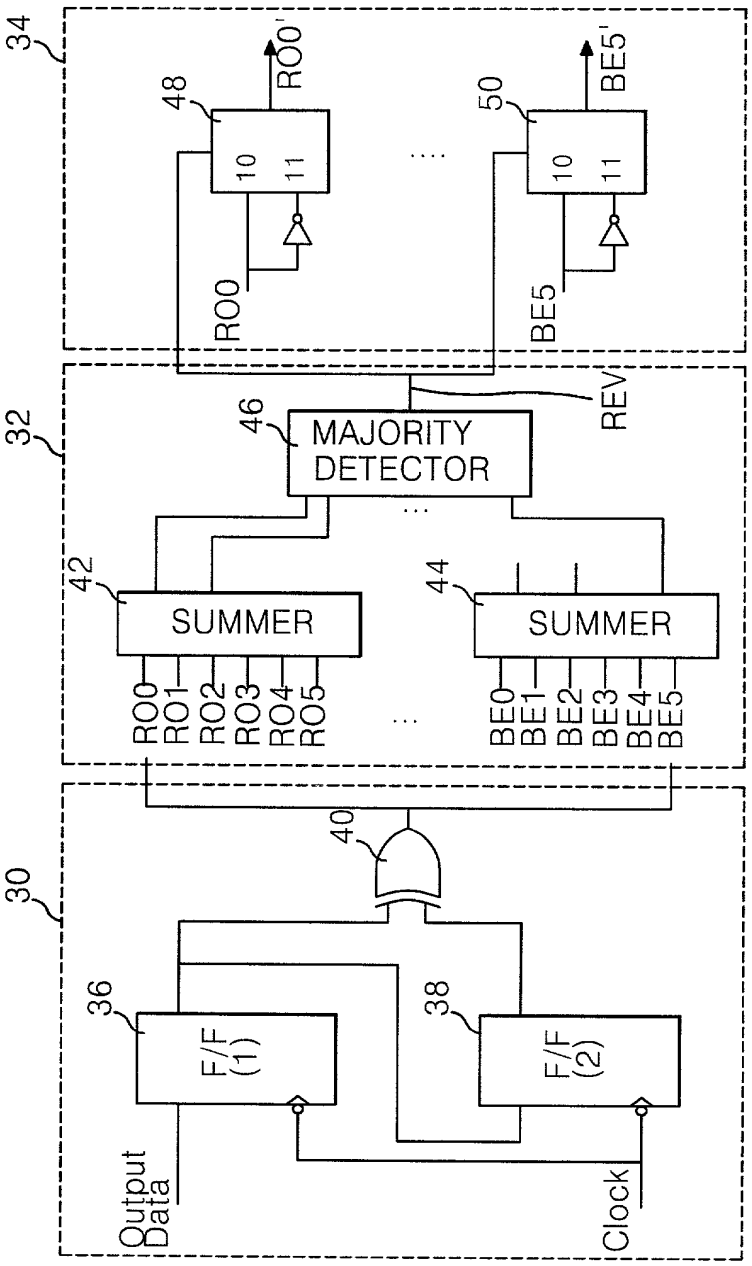


FIG.4B
CONVENTIONAL ART

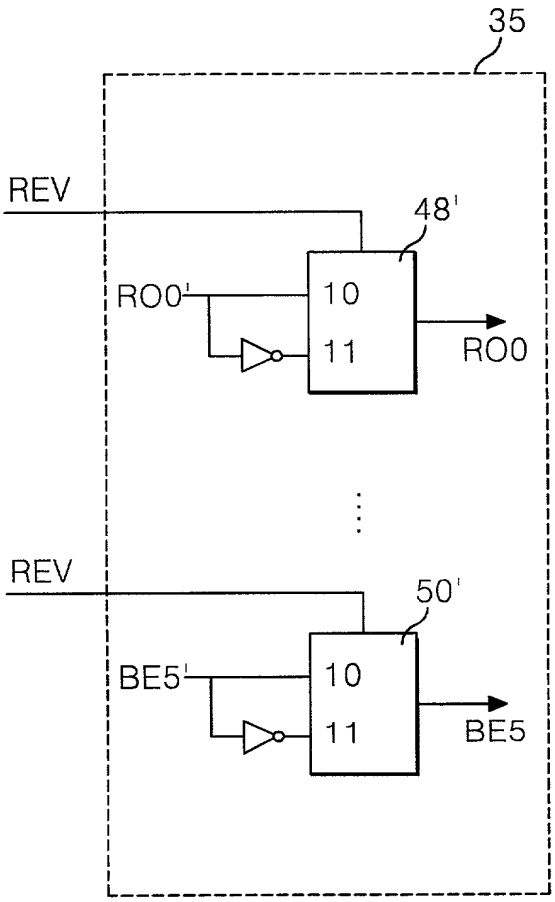


FIG.5
CONVENTIONAL ART

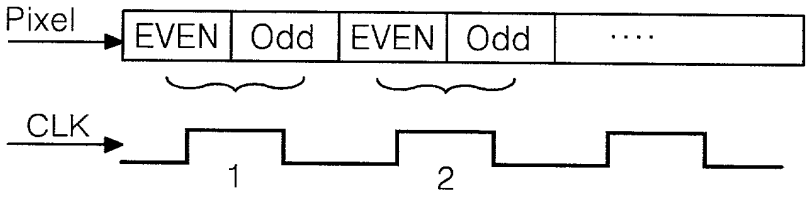


FIG.6

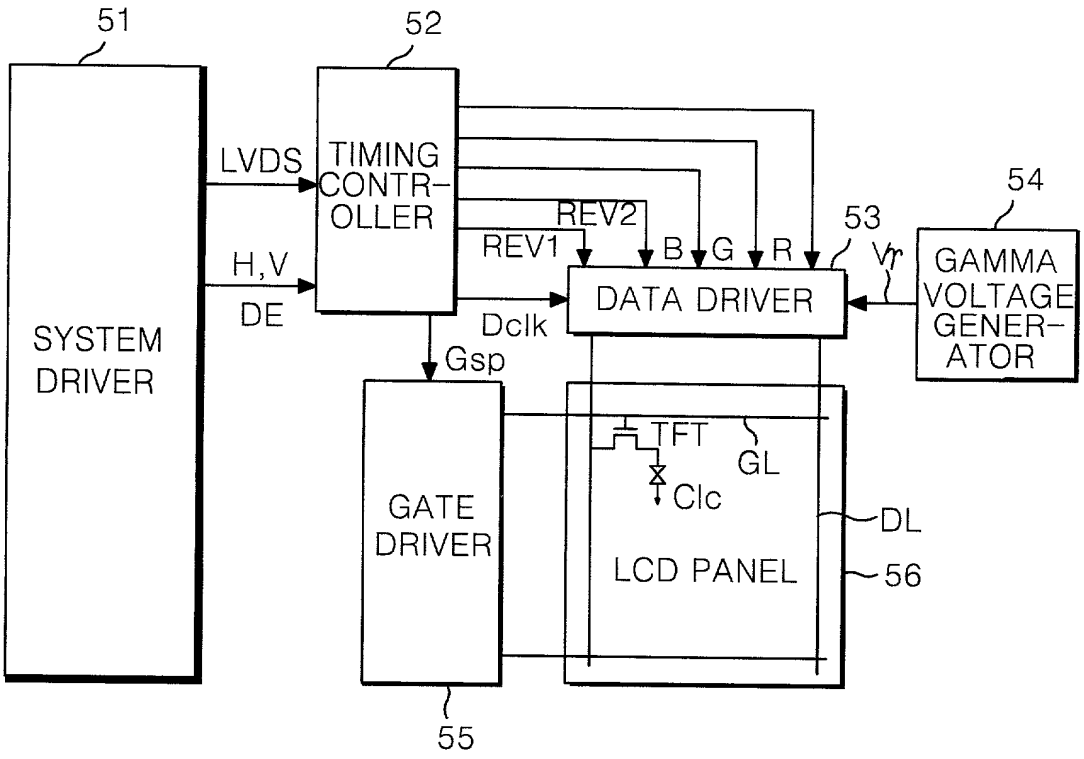

51
52
LVDS
TIMING CONTR-OLLER
54
REV2
53
REV1
B
G
R
Vr
GAMMA VOLTAGE GENER-ATOR
H,V
DE
DATA DRIVER
SYSTEM DRIVER
Dclk
Gsp
TFT
GL
Clc
GATE DRIVER
DL
LCD PANEL
56
55

FIG.7

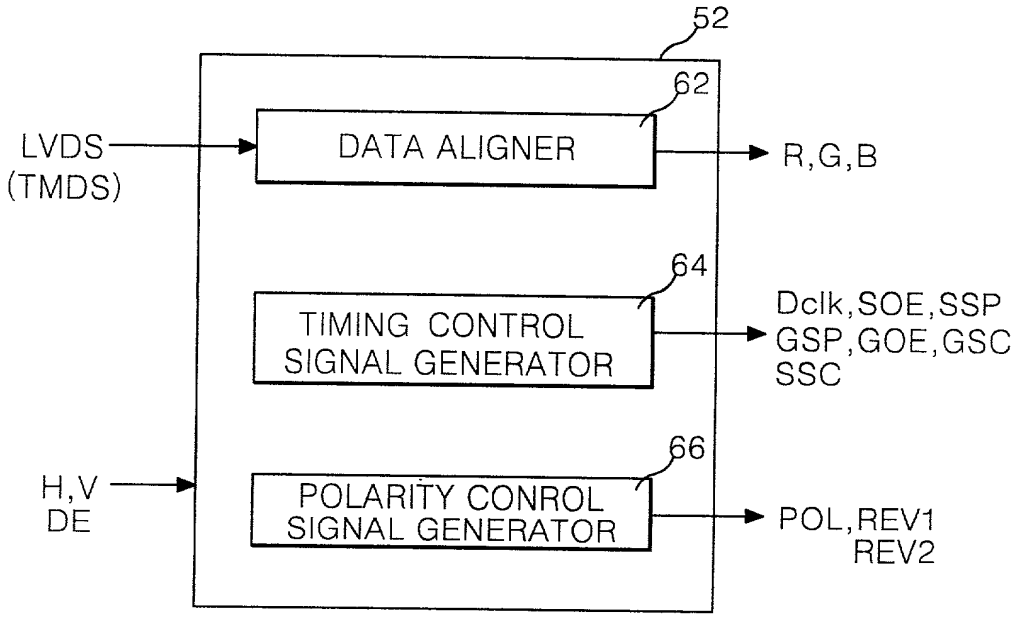

52
62
LVDS
(TMDS)
DATA ALIGNER
R,G,B
64
TIMING CONTROL
SIGNAL GENERATOR
Dclk,SOE,SSP
GSP,GOE,GSC
SSC
66
H,V
DE
POLARITY CONROL
SIGNAL GENERATOR
POL,REV1
REV2

FIG.8A

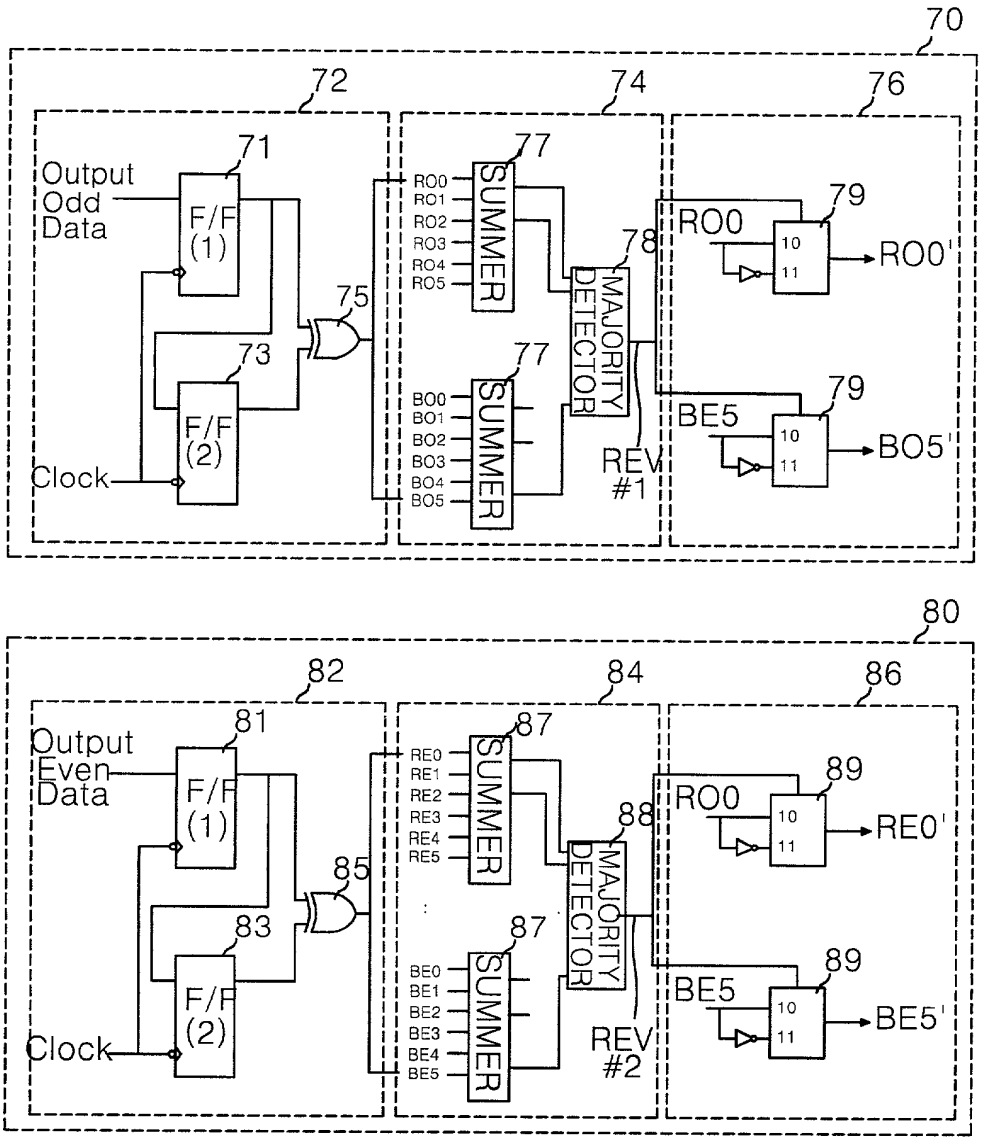

70
72
74
76
71
Output
Odd
Data
F/F
(1)
73
F/F
(2)
Clock
75
77
SUMMER
RO0
RO1
RO2
RO3
RO4
RO5
77
SUMMER
BO0
BO1
BO2
BO3
BO4
BO5
78
MAJORITY
DETECTOR
REV
#1
79
RO0
10
11
RO0'
79
BE5
10
11
BO5'
80
82
84
86
81
Output
Even
Data
F/F
(1)
83
F/F
(2)
Clock
85
87
SUMMER
RE0
RE1
RE2
RE3
RE4
RE5
87
SUMMER
BE0
BE1
BE2
BE3
BE4
BE5
88
MAJORITY
DETECTOR
REV
#2
89
RO0
10
11
RE0'
89
BE5
10
11
BE5'

FIG.8B

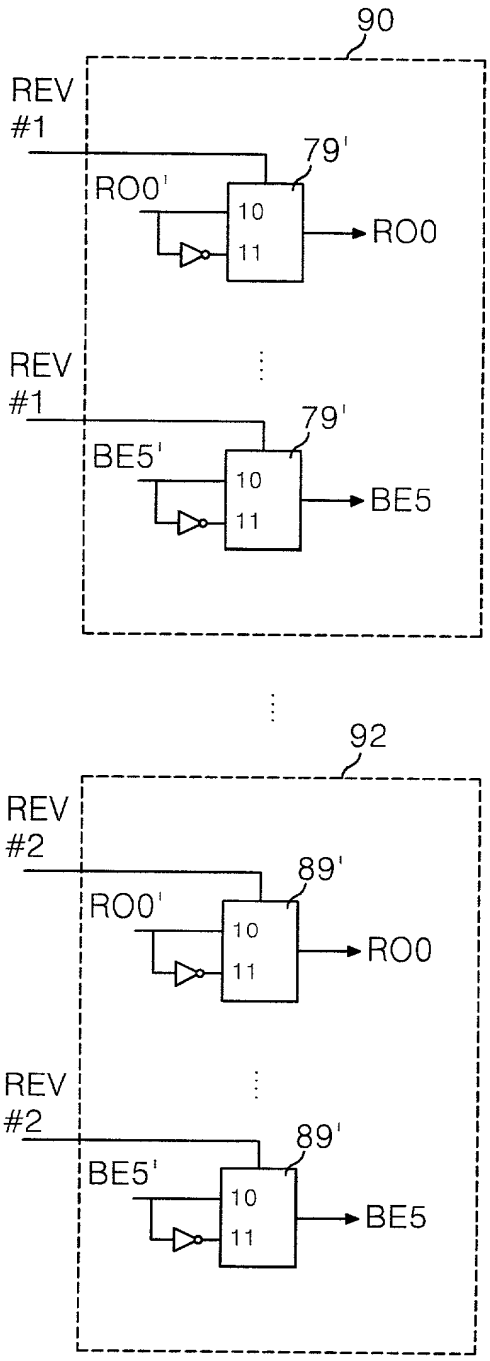

90
REV
#1
79'
RO0'
10
11
RO0
REV
#1
79'
BE5'
10
11
BE5
92
REV
#2
89'
RO0'
10
11
RO0
REV
#2
89'
BE5'
10
11
BE5

FIG.9

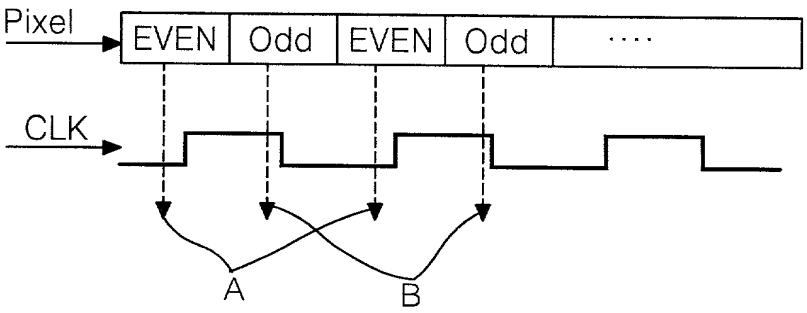


FIG.10

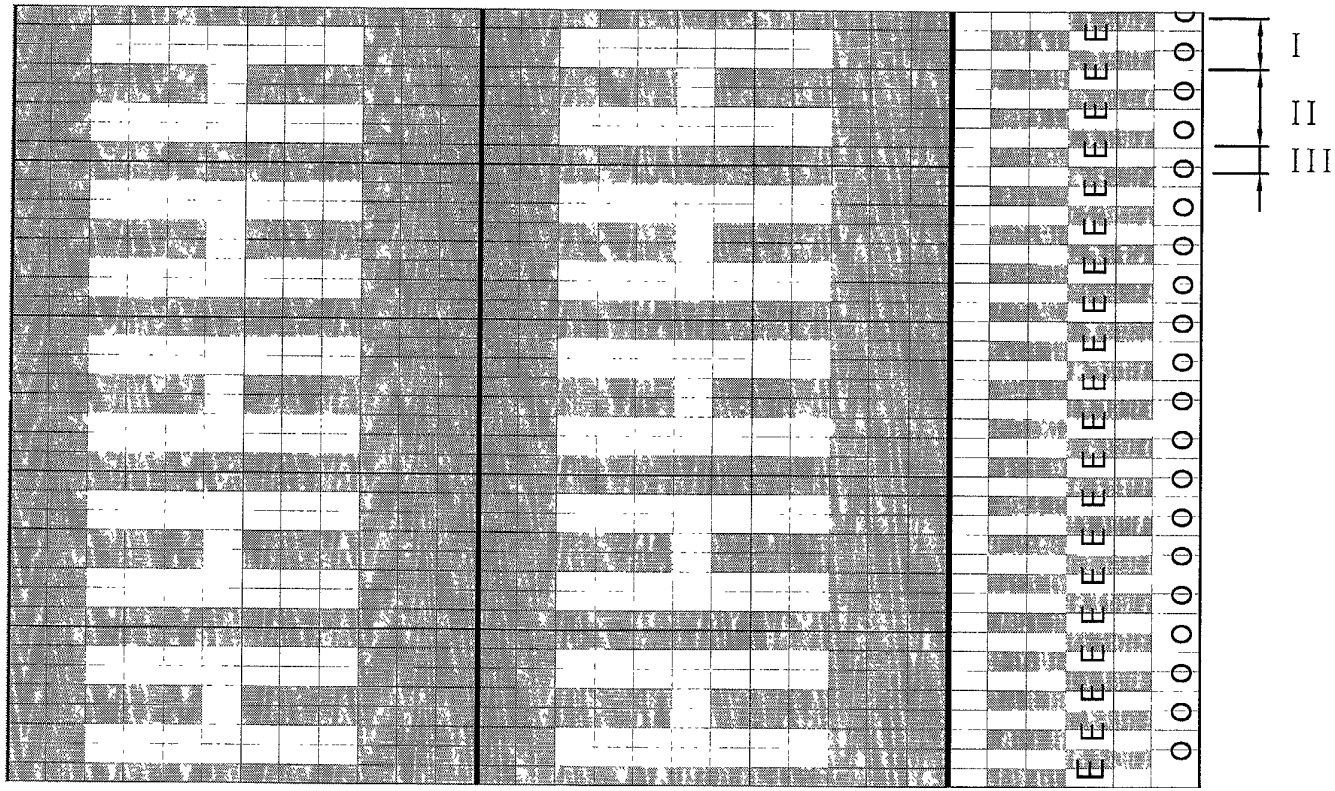


FIG.11

	Dn	Dn-1	Dn-2	Dn-3	Dn-4	Dn-5	Dn-6	Dn-7	Dn-8
REO	1	0	0	0	1	0	0	0	1
RE1	1	0	0	0	1	0	0	0	1
RE2	1	0	0	0	1	0	0	0	1
RE3	1	0	0	0	1	0	0	0	1
RE4	1	0	0	0	1	0	0	0	1
RE5	1	0	0	0	1	0	0	0	1
GE0	1	0	0	0	1	0	0	0	1
GE1	1	0	0	0	1	0	0	0	1
GE2	1	0	0	0	1	0	0	0	1
GE3	1	0	0	0	1	0	0	0	1
GE4	1	0	0	0	1	0	0	0	1
GE5	1	0	0	0	1	0	0	0	1
BE0	1	0	0	0	1	0	0	0	1
BE1	1	0	0	0	1	0	0	0	1
BE2	1	0	0	0	1	0	0	0	1
BE3	1	0	0	0	1	0	0	0	1
BE4	1	0	0	0	1	0	0	0	1
BE5	1	0	0	0	1	0	0	0	1
RO0	0	0	0	1	0	0	0	1	0
RO1	0	0	0	1	0	0	0	1	0
RO2	0	0	0	1	0	0	0	1	0
RO3	0	0	0	1	0	0	0	1	0
RO4	0	0	0	1	0	0	0	1	0
RO5	0	0	0	1	0	0	0	1	0
GO0	0	0	0	1	0	0	0	1	0
GO1	0	0	0	1	0	0	0	1	0
GO2	0	0	0	1	0	0	0	1	0
GO3	0	0	0	1	0	0	0	1	0
GO4	0	0	0	1	0	0	0	1	0
GO5	0	0	0	1	0	0	0	1	0
BO0	0	0	0	1	0	0	0	1	0
BO1	0	0	0	1	0	0	0	1	0
BO2	0	0	0	1	0	0	0	1	0
BO3	0	0	0	1	0	0	0	1	0
BO4	0	0	0	1	0	0	0	1	0
BO5	0	0	0	1	0	0	0	1	0

DATA OUTPUT UPON REV OFF

FIG.12

	Dn	Dn-1	Dn-2	Dn-3	Dn-4	Dn-5	Dn-6	Dn-7	Dn-8
REO	0	1	1	0	0	1	1	1	1
RE1	0	1	1	0	0	1	1	1	1
RE2	0	1	1	0	0	1	1	1	1
RE3	0	1	1	0	0	1	1	1	1
RE4	0	1	1	0	0	1	1	1	1
RE5	0	1	1	0	0	1	1	1	1
GE0	0	1	1	0	0	1	1	1	1
GE1	0	1	1	0	0	1	1	1	1
GE2	0	1	1	0	0	1	1	1	1
GE3	0	1	1	0	0	1	1	1	1
GE4	0	1	1	0	0	1	1	1	1
GE5	0	1	1	0	0	1	1	1	1
BE0	0	1	1	0	0	1	1	1	1
BE1	0	1	1	0	0	1	1	1	1
BE2	0	1	1	0	0	1	1	1	1
BE3	0	1	1	0	0	1	1	1	1
BE4	0	1	1	0	0	1	1	1	1
BE5	0	1	1	0	0	1	1	1	1
RO0	1	1	1	1	1	1	1	0	0
RO1	1	1	1	1	1	1	1	0	0
RO2	1	1	1	1	1	1	1	0	0
RO3	1	1	1	1	1	1	1	0	0
RO4	1	1	1	1	1	1	1	0	0
RO5	1	1	1	1	1	1	1	0	0
GO0	1	1	1	1	1	1	1	0	0
GO1	1	1	1	1	1	1	1	0	0
GO2	1	1	1	1	1	1	1	0	0
GO3	1	1	1	1	1	1	1	0	0
GO4	1	1	1	1	1	1	1	0	0
GO5	1	1	1	1	1	1	1	0	0
BO0	1	1	1	1	1	1	1	0	0
BO1	1	1	1	1	1	1	1	0	0
BO2	1	1	1	1	1	1	1	0	0
BO3	1	1	1	1	1	1	1	0	0
BO4	1	1	1	1	1	1	1	0	0
	Dn	Dn-1	Dn-2	Dn-3	Dn-4	Dn-5	Dn-6	Dn-7	Dn-8

DATA OUTPUT UPON REV ON

FIG.13

	Dn	Dn-1	Dn-2	Dn-3	Dn-4	Dn-5	Dn-6	Dn-7	Dn-8
REO	1	1	1	1	1	1	1	1	1
RE1	1	1	1	1	1	1	1	1	1
RE2	1	1	1	1	1	1	1	1	1
RE3	1	1	1	1	1	1	1	1	1
RE4	1	1	1	1	1	1	1	1	1
RE5	1	1	1	1	1	1	1	1	1
GE0	1	1	1	1	1	1	1	1	1
GE1	1	1	1	1	1	1	1	1	1
GE2	1	1	1	1	1	1	1	1	1
GE3	1	1	1	1	1	1	1	1	1
GE4	1	1	1	1	1	1	1	1	1
GE5	1	1	1	1	1	1	1	1	1
BE0	1	1	1	1	1	1	1	1	1
BE1	1	1	1	1	1	1	1	1	1
BE2	1	1	1	1	1	1	1	1	1
BE3	1	1	1	1	1	1	1	1	1
BE4	1	1	1	1	1	1	1	1	1
BE5	1	1	1	1	1	1	1	1	1
RO0	0	0	0	0	0	0	0	0	0
RO1	0	0	0	0	0	0	0	0	0
RO2	0	0	0	0	0	0	0	0	0
RO3	0	0	0	0	0	0	0	0	0
RO4	0	0	0	0	0	0	0	0	0
RO5	0	0	0	0	0	0	0	0	0
GO0	0	0	0	0	0	0	0	0	0
GO1	0	0	0	0	0	0	0	0	0
GO2	0	0	0	0	0	0	0	0	0
GO3	0	0	0	0	0	0	0	0	0
GO4	0	0	0	0	0	0	0	0	0
GO5	0	0	0	0	0	0	0	0	0
BO0	0	0	0	0	0	0	0	0	0
BO1	0	0	0	0	0	0	0	0	0
BO2	0	0	0	0	0	0	0	0	0
BO3	0	0	0	0	0	0	0	0	0
BO4	0	0	0	0	0	0	0	0	0
BO5	0	0	0	0	0	0	0	0	0

DATA OUTPUT UPON REV 1,2 DRIVING (DC LEVEL)

FIG.14A

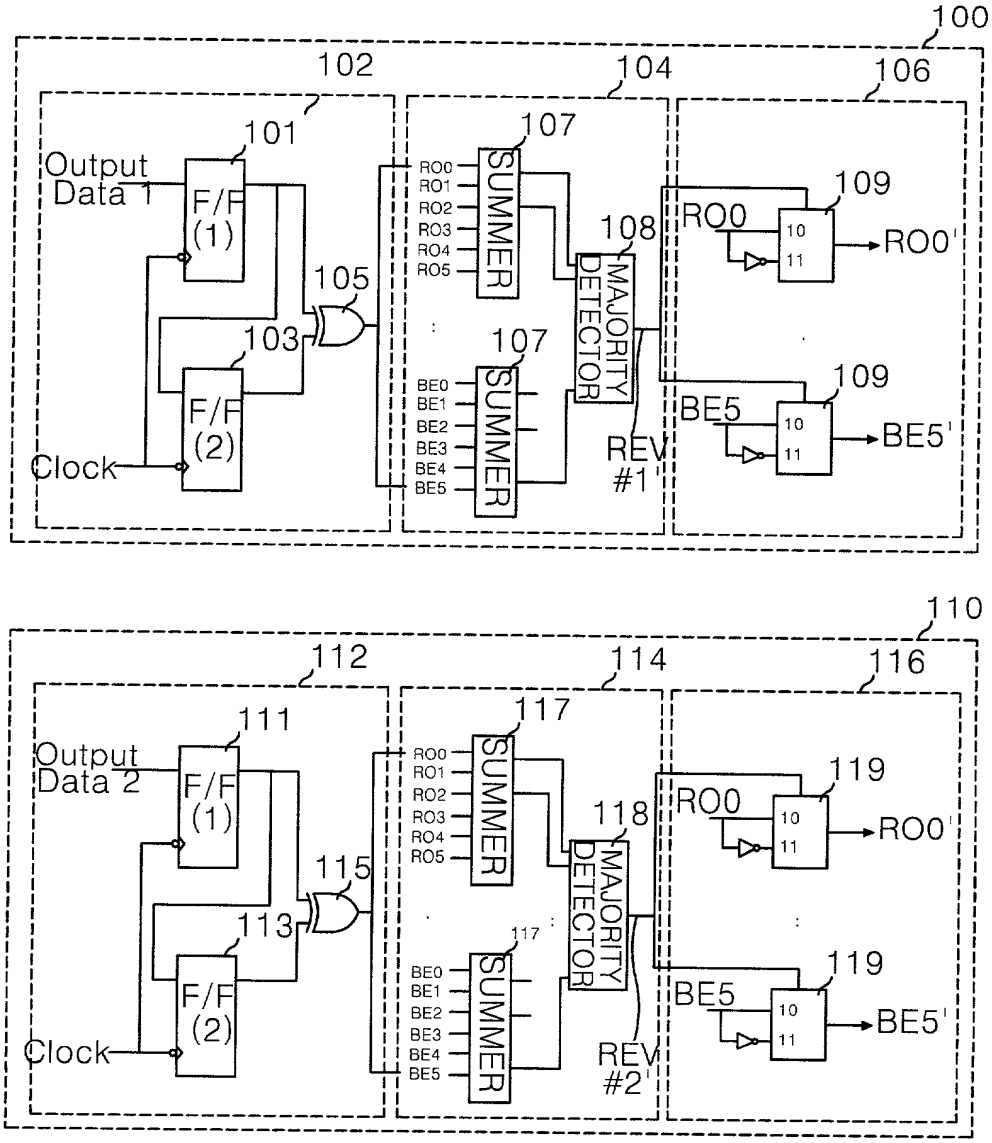
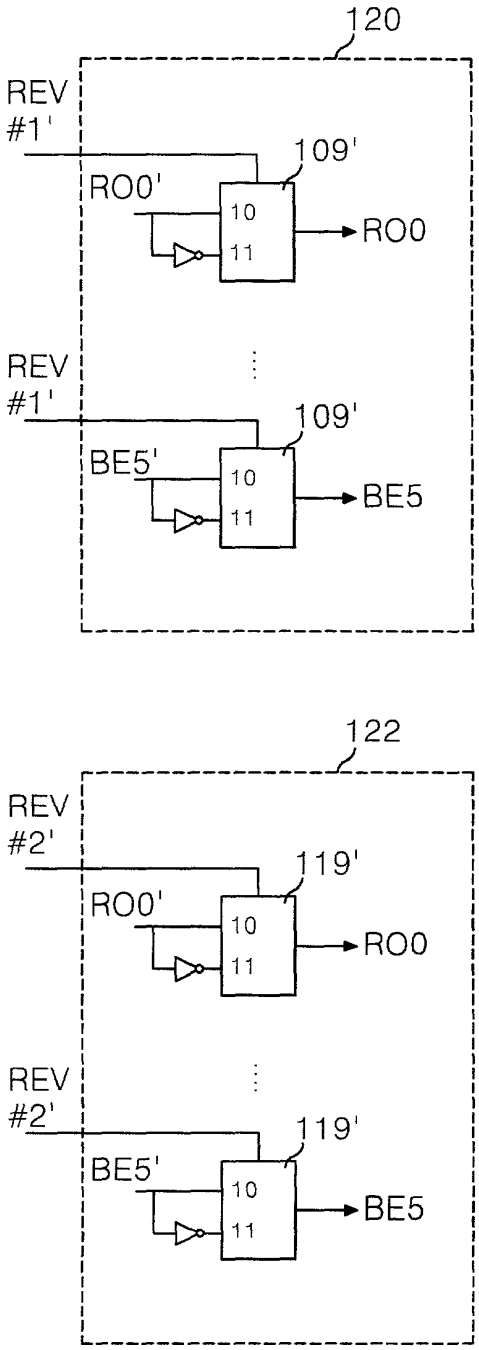

100
102
104
106
101
Output Data 1
F/F (1)
103
F/F (2)
Clock
105
107
RO0
RO1
RO2
RO3
RO4
RO5
SUMMER
107
BE0
BE1
BE2
BE3
BE4
BE5
SUMMER
108
MAJORITY DETECTOR
REV #1'
109
RO0
10
11
RO0'
109
BE5
10
11
BE5'
110
112
114
116
111
Output Data 2
F/F (1)
113
F/F (2)
Clock
115
117
RO0
RO1
RO2
RO3
RO4
RO5
SUMMER
117
BE0
BE1
BE2
BE3
BE4
BE5
SUMMER
118
MAJORITY DETECTOR
REV #2'
119
RO0
10
11
RO0'
119
BE5
10
11
BE5'

FIG.14B


120
REV #1'
109'
RO0'
10
11
RO0
REV #1'
109'
BE5'
10
11
BE5
122
REV #2'
119'
RO0'
10
11
RO0
REV #2'
119'
BE5'
10
11
BE5